High Speed FPGA Implementation of FIR Filters for DSP Applications

**ABSTRACT**

Signal processing ranks among the most demanding applications of digital design concepts. It is a mature technology domain wherein the demands for enhanced performance and reduced resource utilization have risen exponentially over the years. Field Programmable Gate Array (FPGA) design technology has becoming the preferredplatform for evaluating and implementing signal processing algorithms. The advantages of the FPGA approach to digital filter implementation include higher sampling rates than are available from traditional DSP chips, lower costs than an application specific integrated circuit (ASIC) for moderate volume applications, and more flexibility than the alternate approaches. Since many current FPGA architectures are in-system programmable, the configuration of the device may be changed to implement different functionality if required. This paper describes an approach to the implementation of digital filter based on field programmable gate arrays (FPGAs) which is flexible and provides performance comparable or superior to traditional approaches, lowpower, area-efficient re-configurable digital signal processing architecture that is tailored for the realization of arbitrary response Finite impulse response (FIR) filters.

**LANGUAGE USED:**

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis